Comparison between MCML and CMOS Digital Circuits For Using ADS Simulation

Dr.Luqman Sufer Ali
Department of Computer Engineering,
College of Engineering, University of Mosul
Luqmansufer@yahoo.com

Zahra RafidMahmod
Department of Electrical Engineering,
College of Engineering, University of Mosul
albadrane_2003@yahoo.com

Abstract:

In this paper, a comparison is done between MOS Current Mode Logic (MCML) and Complementary metal Oxide Semiconductor (CMOS) circuits operating in low power application. It is found that MCML logic circuits exhibit a decrease in delay and so decrease in overall power delay product compared with CMOS circuits. The tested inverter, D-latch NAND/AND, XOR/XNOR are optimized for low power and high-speed operation, according to the simulation of the circuits for lower voltage operating at data rate 2.5 GHz. This simulation is done using Advanced Design System(ADS2009).From the results shown it is seen that the MCML logic circuits reveal high efficiency and good performance at low power and high speeds which makes them to be more capable for application in the integrated circuits with high density.

مقارنة بين دوائرMCML ودوائر CMOS المنطقية باستخدام ADS في المحاكاة

زهراء رافد محمود
قسم الهندسة الكهربائية - كلية الهندسة
جامعة الموصل- الموصل-العراق
albadrane_2003@yahoo.com

د. لقمان سفر علي
قسم الهندسة الكهربائية- كلية الهندسة
جامعة الموصل- الموصل-العراق
Luqmansufer@yahoo.com

ألخلاصة

في تطبيقات القدرة الواطئة فقد لوحظ ان دوائر CMOS ودوائرMCML في هذا البحث تمت المقارنة بين دوائر المنطقية فقد تم فحص كل منCMOS قليلة مقارنة مع دوائر ال المنطقية تمتاز بزمن PDP , (T_B) تأخيرMCML عند قدرات واطئةوسرعة تشغيل عالية وفقالمحاكاة-XOR/NOR,NAND/AND,D دوائر القالب في المحاكاةADS2009 لقد تم استخدام برنامج الGHz 2.5.هذه الدوائر عند التشغيل latch,Inverter بفولتيات واطئة وبتردد المنطقية اظهرت كفاءة عالية في الاداء بقدرات واطئة وبسرعاتMCMLبالحاسبة. حيثتبينمنخلالالنتائجباندوائرعالية مما يؤهلها ان تكون مرشحة في تطبيقات الدوائر المتكاملة ذات الكثافة العالية جدا.

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I. Introduction

With the rapid increase in transmission speeds of communication systems, the demand for very high-speed low-power VLSI circuits is on the rise. The development of these high-speed circuits has three main driving forces:

1. higher levels of integration to provide higher performance at lower cost.
2. the use of popular VLSI technologies such as CMOS.
3. the ability to provide low-power system-on-chip implementations[1].

MCML is a logic style that is widely used in high-speed circuits [2].
This logic style was first implemented using bipolar transistor, but with the advance in CMOS technology and the scaling-down of its feature size, MOS implementation of CML became attractive. Although a lot of research work was conducted on bipolar CML and modeling its delay, MCML did not receive the same interest.
Over the past few years, MCML has been used extensively to realize Gbps multiplexers and demultiplexers for optical transceivers. The ultimate goal of that work was to have a fully integrated optical transceiver. However, high power dissipation poses as an obstacle in these designs [3].
Although the performance of CMOS technologies improves notably with scaling, conventional CMOS circuits cannot simultaneously satisfy the speed and power requirements of these applications. Moreover, conventional CMOS circuits generate significant supply noise, thus hindering the on-chip integration of sensitive analog and digital circuits. MOS current-mode logic (MCML) has emerged as a logic style that can achieve the much needed high speeds while consuming less power than conventional CMOS circuits at these high frequencies [1].
The traditional static-CMOS logic circuit style faces a couple of problems when used for achieving GHz range speed in current deep submicron technologies. The signal integrity problem, due to the large magnitude of the digital signals (both as voltage and as current) and to the single-wire communication, is inherent to the static-CMOS operation. Signal integrity issues like cross-talk noise, cross-talk delay, substrate noise, and power supply noise become complex to address in a design flow based on the static-CMOS logic circuit style[4].
MCML is widely used in high-speed applications, e.g., optical communication transceivers. MCML circuits are characterized by their low supply noise generation and high noise immunity, thus enabling the integration of analog and digital blocks on the same chip. However, MCML designers face a tough and complex problem in designing MCML circuits because the performance and proper operation of MCML is a function of numerous design parameters [1].
Compared to conventional CMOS logic, MCML dissipates constant static power and requires techniques more analogous to analog design. However, MCML requires smaller dynamic power than that of the conventional logic because of the smaller output swings. The reduced output swing and faster switching makes MCML a promising candidate for certain mixed-signal applications. The constant supply currents, lower cross talk between the analog and the digital circuits of MCML improves the accuracy of mixed-mode systems. Additional efficiency can be obtained using more than one level of logic [5].

II. MOS Current Mode Logic(MCML) overview*:*

III. The conventional MCML circuit consists of three main components which include a differential pull-down network(PDN), a bias source and a pull-up load circuit as shown in Fig(1). The PDN employs differential n MOS transistor pairs (M1, M2) and performs the logic function [3].

The inputs to the pull down network (PDN) are fully differential. In other words, the true and complement off all logical inputs must be presented to the gate. The PDN can implement any logic function but must have a definite value for all possible input combinations. In general,the design of the MCML pull down network is similar to other differential logic styles such as differential cascade voltage switch logic (DCVSL) or differential split-level logic (DSL). Unlike DCVSL or DSL, the pull down network in MCML circuits is regulated by a constant current source [6].

The constant current source determines the source current,I_{ss} whereas the pMOS load determines the voltage swing. MCML circuit works on the principle of current steering. [6] The pull down network steers the currentI_{ss} to one of pMOS transistors based upon the logic function being implemented [6].

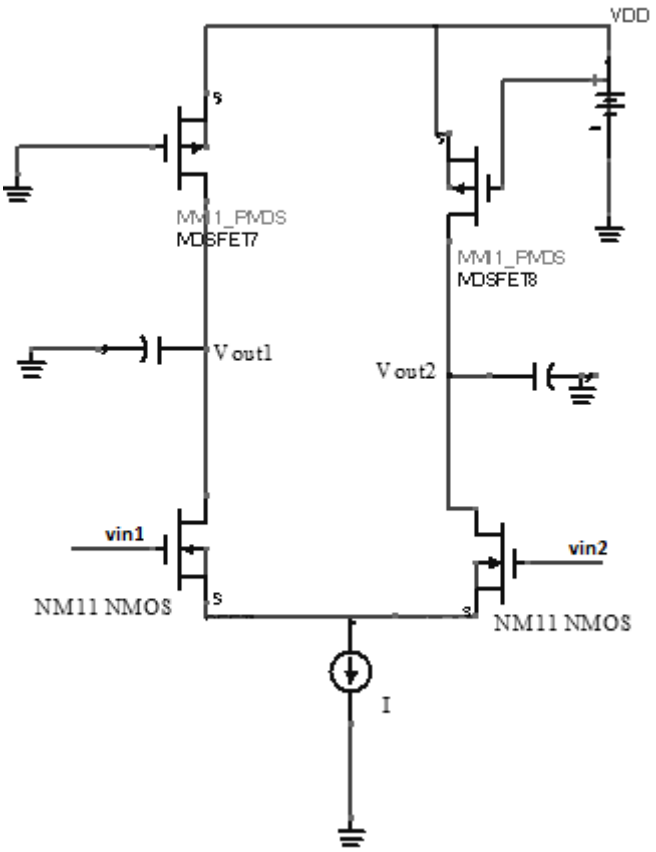


Fig (1) Conventional MCML Inverter

The differential input voltage,

$$V_{id} = V_{i1} - V_{i2} \quad \ldots(1)$$

is high (low), the NMOS source-coupled pair steers the bias current, I_{ss} to the drain of M1 (M2), thereby generating a low (high) outputvoltage

$$V_0 = V_{01} - V_{02} \quad \ldots(2)$$

The output voltage is equal to $-R_{pMOS}I_{ss}(+R_{pMOS}I_{ss})$. pMOS load has an advantage of smaller area than passive resistances, but deviates from the linear behavior, especially at high speeds. It also adds an extra capacitance to the total output load capacitance and degrades the transient response of the circuit as a consequence [7].

IV. Analysis of MCML design parameters and variables:

MCML designers face a tough and complex problem in designingMCML circuits because the performance and proper operation of MCML circuit is a function of numerous design parameters. So that MCML designers need to fully understand the different tradeoffs associated with each of the design parameters involved in the design process. The design parameters for a typical MCML circuit are the circuit delayt_d, total power dissipationP_d,

voltage swing ΔV, voltage gain A_v , noise margin NM, voltage swing ratio VSR ,and signal slope ratio SSR[1].

a. Total circuit delay (t_d):

Since MCML circuits experience small voltage swings of ΔV,a small-signal model can be used to approximate their behavior.The delay of MCML depends on AV, $I_s$and the load capacitance.[3] Usingfirst-order circuit analysis,t_d is approximated by[1]

$$t_d = 0.69RC \quad \text{... (3)}$$

b. Power Dissipation(P_d):

MCML circuits consume static power because of the use ofa constant current source, while dynamic power dissipation is ignorable with respect to static power.
from which it is deduce that the power dissipation in MCML is constant with the frequency, unlike conventional CMOS, thus suggesting dominant static power dissipation in MCML circuits. Therefore,P_d in MCML is given by:[1]

$$P_d = V_{DD} \times I \quad \text{... (6)}$$

c. Voltage Swing (ΔV):

The voltage swing ΔV *of MCML circuits is expressed as:*

$$\Delta V = I \times R \quad \text{... (7)}$$

ΔV is an important parameter that links power dissipation withperformance because circuits with the same ΔV and $C_L$must sink alarger *I*to have shortert_d . In order to minimize the effectof external noise sources on the input/output signals, a lowerbound of 0.1 V with aV_{DD} of 1.8V is used for ΔV. The upperbound onΔV is determined by the saturation condition of$M_1(\Delta V \leq V_{th_1})$[1].

d. DC Voltage Gain (A_v):

The dc voltage gain A_v is defined as the voltage gain at thevoltage mid-swing. A_v is a key parameter in controlling the circuitregeneration and stability. For single-level MCML, A_v isexpressed as :

$$A_v = g_{m_1} R = \Delta V \sqrt{\mu_n C_{ox} \frac{W_{eff1}}{L_{eff1\,I}}} \quad \text{--------(8)}$$

Where $g_{m_1}$is the transconductance of M_1,C_{ox} is the oxide capacitance of the MOS, $\mu_n$is the electron mobility, and $W_{eff1}$and $L_{eff1}$are the effective width and length of M_1,respectively.Since MCML circuits have high noise immunity andgenerate small switching noise, thus they can function properlyat a small margin above unity gain.To compromise betweenthe performance and circuit regeneration/stability a 40% marginabove unity is used in this work for$A_v(A_v \geq 1.4)$. [1]

e. Noise Margin (NM):

Noises attack the integrity of digital signals and when they becametoo large they can even destroy the logical information carried by these signals. The amount of noise that a gate can tolerate without compromising the logical functionality is usually termed asnoise-margin and is dependent on noise type .For the case of low-swing digital signals, we believe that also the on-chip process variations are an important noise source: the static noise associated with the on-chip process variations can have similar deleterious effects on the logic state of a latch as

the dynamic noises. Especially for MCML, that resembles analog operation and thus may seem more susceptible to noises than static-CMOS' logic, it is important to study how much noise a gate can tolerate without compromising the logical functionality and which factors contribute to the noise robustness [4].

It is significant to achieve a sufficiently large noise margin in MCML circuits because of the use of reduced voltage swings. However, the high noise immunity of MCML circuits allows designers to accept small values for *NM*, with the theoretical maximum (when A_v is very large) beingΔV.Practically, a *NM* of 40%ΔV is sufficient to ensure proper circuit operation withoutdegrading the performance.For a single-level MCML circuit, *NM* is given by:

$$NM = \Delta V \frac{\sqrt{4A_v^2 - 1 - \sqrt{8A_v^2 + 1}}}{A_v^2\sqrt{2}} \times \left(\frac{\sqrt{4A_v^2 - 1 + \sqrt{8A_v^2 + 1}}}{2\sqrt{2}} - 1 \right) \quad \ldots (10)$$

In order to have a noise margin larger than $0.4 \times \Delta V$ in single-level MCML circuits, A_v must be larger than 2 [1].

f. Voltage Swing Ratio(VSR):

Ideally, MCML circuits act as perfect current switches, steering all of the current generated by $M_s$to the ON branch. However, in reality, a portion of *I* flows through the OFF branch, thus reducing the output voltage swing of the circuit. The problem is even more complicated in subsequent cascaded circuits as the quality of current switching will continue to drop, resulting in a chain of circuits having a continually degrading voltage swing as the current in the OFF branch is pushed to a non-restoring value. To overcome this problem, the current flowing through the OFF branch is constrained to a small percentage of the total current *I*. The voltage swing ratio VSR is defined as the ratio between the current in the ON branch I_{on} to the total current. A near-unity value for VSR is required to have an almost ideal current switching capability. However, increasing VSR necessities increaseW_1 or decreasing *I*, which results in degrading the circuit performance by increasing the load capacitance or increasing the total power dissipation, respectively. To best balance between these effects, VSR above 95% is used, which is sufficient to have enough current switching capabilities in MCML. For single-level MCML, $I_{on}$is the saturation current of M_1[1].

g. Signal Slope Ratio (SSR):

The total delay of cascaded MCML circuits depends on two main factors: the propagation delay t_d and the shape of theoutput waveform of each circuit.Since speed is an importantissue in MCML design, a metric is needed to ensure that theiroutput response will not have long rise/fall times t_{rf} with respect to t_d . The signal slope ratio SSR is defined as the ratiobetween $t_d$to t_{rf} , which should be kept as small as possible tohave a good output waveform [1].

h. Design of the Differential Pair Transistors (W_n, L_n, W_p, L_p):

Increasing L_1 prolongs t_d by adding up to the parasitic capacitance of M_1.Using the minimum technology feature size for the length dimensions increases the impact of possible process variations (the effect of process variations is inversely proportional to the dimension).Hence,$L_n L_p$ are kept fixed at a nonminimum channel length, which is double the minimum feature size of the technology ($L = 2L_{min}$).Using large W_n values increases A_v , but on the other hand,adds up to the load capacitance, which in turn results in longer delays.

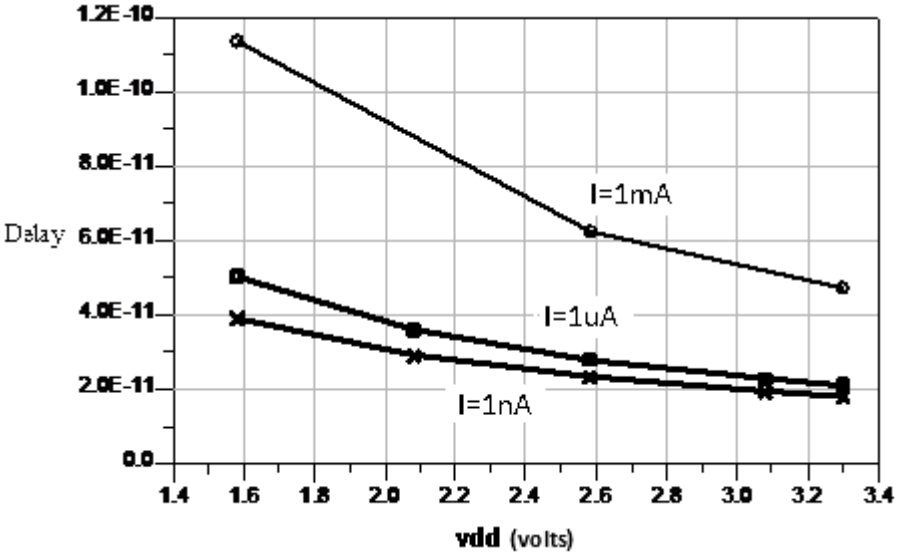
Thus, a compromise between A_v and t_d should be reached to provide a reasonable size for W_n. In the MCML, latch,W_p does not affect any of the circuit parameters and is selected as double the minimum size (for the same reasoning above).W_p is designed to be equal toW_n[1].

V. Results and Discussion:

a. Comparison between CMOS and MCML:

The most important different between CMOS and MCML is that MCML dissipates less power than CMOS in high frequencies application, while providing an analog friendly environment. Although the performance of CMOS technologies improves notably with scaling, conventional CMOS circuits cannot simultaneously satisfy the speed and power requirements of these applications. Moreover, conventional CMOS circuits generate significant supply noise, thus hindering the on-chip integration of sensitive analog and digital circuits. MOS current-mode logic (MCML) has emerged as a logic style that can achieve the much needed high speeds while consuming less power than conventional CMOS circuits at these high frequencies. [1]MCML circuits are characterized by their low supply noise generation and high noise immunity, thus enabling the integration of analog and digital blocks on the same chip. Static synchronous CMOS circuits have increasingly difficult challenges to overcome in terms of clock skew and switching noise in ultra-deep-submicron design. Advantageous characteristics of MCML are lower crosstalk (In addition, the steady current source of MCML reduces the power supply fluctuations and noise. This property and the small output voltage swing of MCML gates help to minimize cross talk between adjacent digital and analog blocks in a mixed-signal environment.) owing to the reduced output voltage swing. This has made asynchronous circuit design an increasingly practical alternative. [1,3]

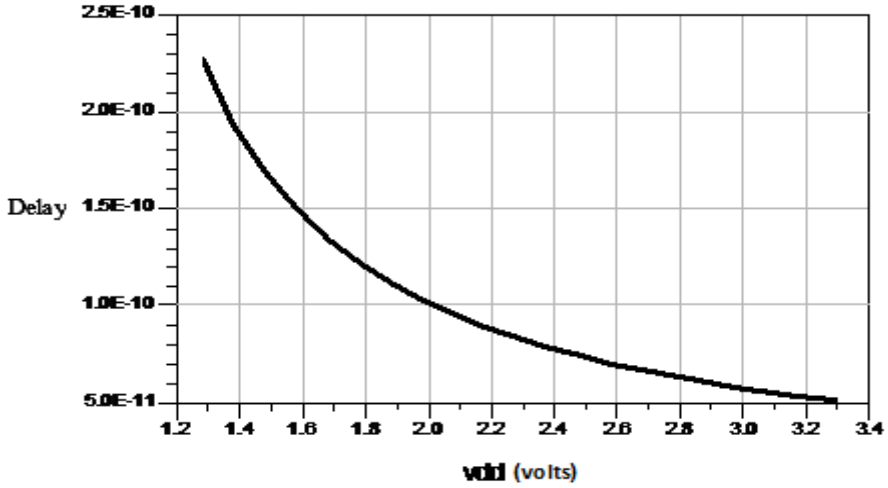
The delay characteristics of MCML when I=1mA,1uA,1nAand CMOS inverter are shown in fig (2) and fig(3),



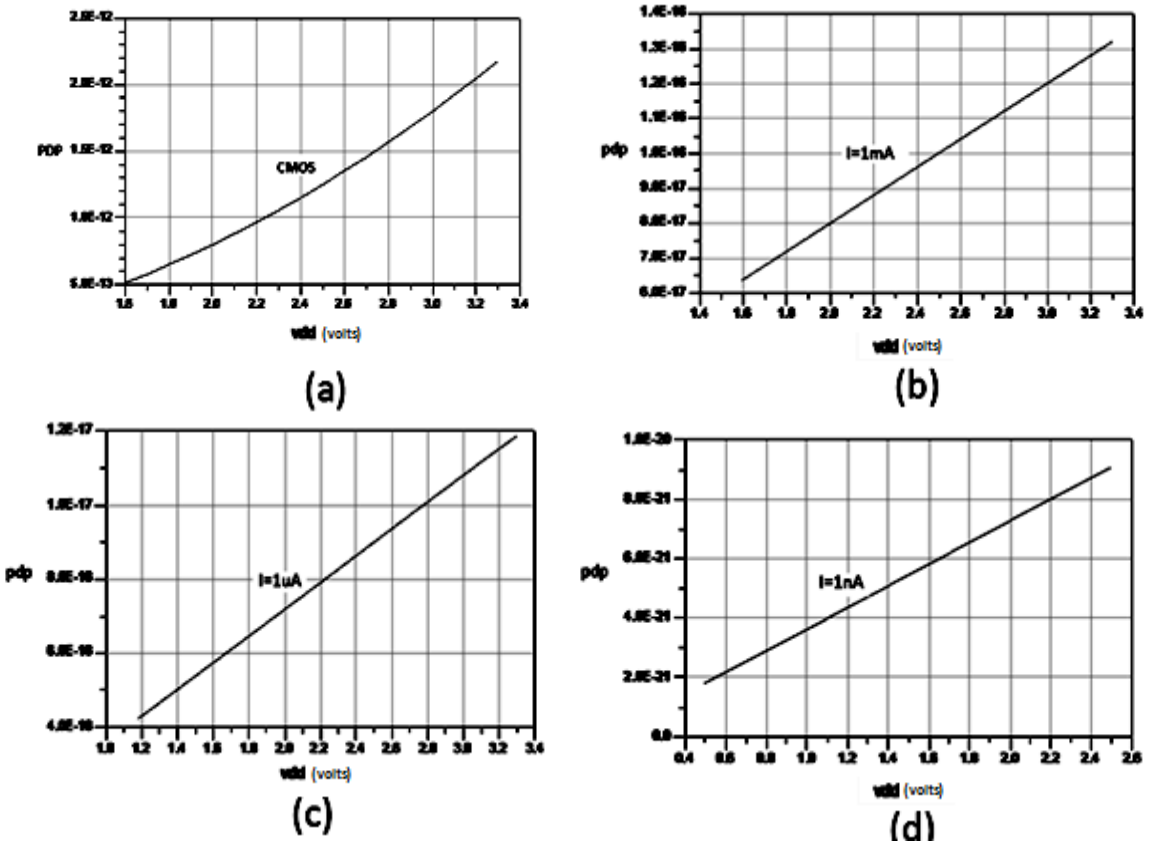
Fig(2) Delay versus vdd (volts)plot of MCML Inverter when I=1mA,1uA,1nA

It can be observed that when the vdd of pull-up transistors in MCML is scaled up, the delay will decrease which is contrary to that of static CMOS logic inverter. In sub-threshold region, the static CMOS inverter shows a drastic increase in delay with decrease in supply voltage whereas in the case of MCML the average delay still decreases. MCML topology finds application where high speed is our primary concern. MCML logic circuits operating in sub-threshold region for combines both low power and lower delay results in lower PDP contrary

to CMOS logic circuits. MCML logic gates are advantageous over CMOS logic gates in the applications where delay is the main concern. And in the sub-threshold region of operation, both the gate topologies have comparable PDP.[8]

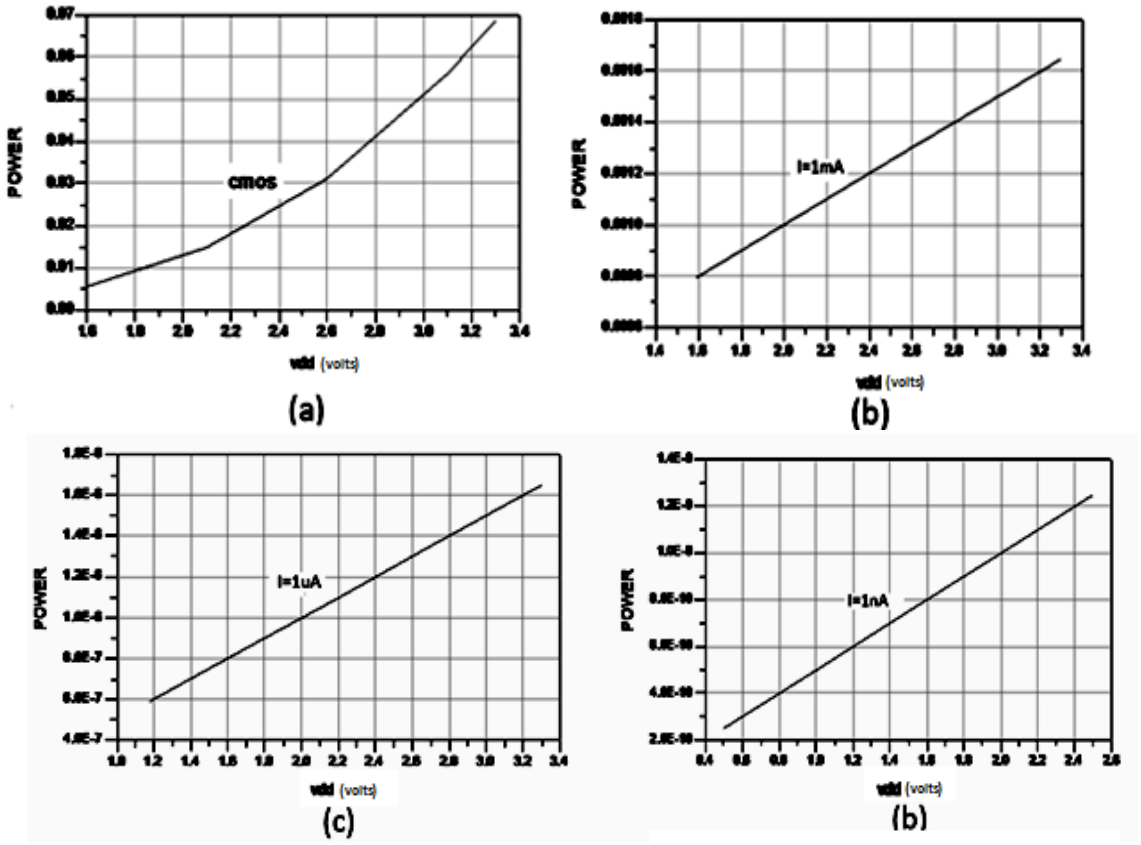


Fig(3) Delay versus vdd(volts)plot of static CMOS Inverter



Fig(4)PDP versus vdd(volts) plot of static CMOS and MCML Inverter for different tail current

Fig(4) shows the relation between power -delay product(PDP) and the power supply voltage (vdd). It can be observed that when vdd is scaled up , the PDP increases in MCML and CMOS . Also PDP will decrease with decreasing the current bias for MCML inverter.



Fig(5) power dissipated versus vdd (volts) plot of static CMOS and MCML Inverter for different tail current

The power dissipated for MCML for different tail current (I=1mA ,1uA ,1nA) and Cmos inverter are shown in fig (5) for 0.18cmos technology. It can be observed that when the vdd of pull-up transistors in MCML is scaled up , the power also increases but it is less compared to power for static CMOS logic inverter and it is noted that when current bias for MCML inverter decreases the PDP decreases also.
The simulation results for CMOS and MCML logic gates (2-Input EXOR, 2-InputAND and D-LATCH Gate) are listed in Table I ,Table II, Table III and the results are compared VDD voltages namely at two vdd=1.8V and vdd = 3V). Results consist of various performance measures such as delay, PDP and dissipated power.

Table I Performance measures for MCML and Cmos AND logic gates

AND GATE	Vdd=1.8v			Vdd=3v		
	Cmos	MCML (I=1mA)	MCML (I=1uA)	Cmos	MCML (I=1mA)	MCML (I=1uA)
Delay(sec)	$2.7e^{-10}$	$9.952e^{-11}$	$5.2e^{-11}$	$2.412e^{-10}$	$5.529e^{-11}$	$4.5e^{-11}$
PDP(joule)	$1.8e^{-14}$	$2.22e^{-14}$	$3.22e^{-17}$	$3.66e^{-14}$	$3.66e^{-14}$	$5.28e^{-17}$
Power Dissipated(watt)	$8.34e^{-4}$	$4.111e^{-4}$	$4.6e^{-7}$	0.0015	$6.775e^{-4}$	$6.5e^{-7}$

Table II Performance measures for MCML and Cmos XOR logic gates

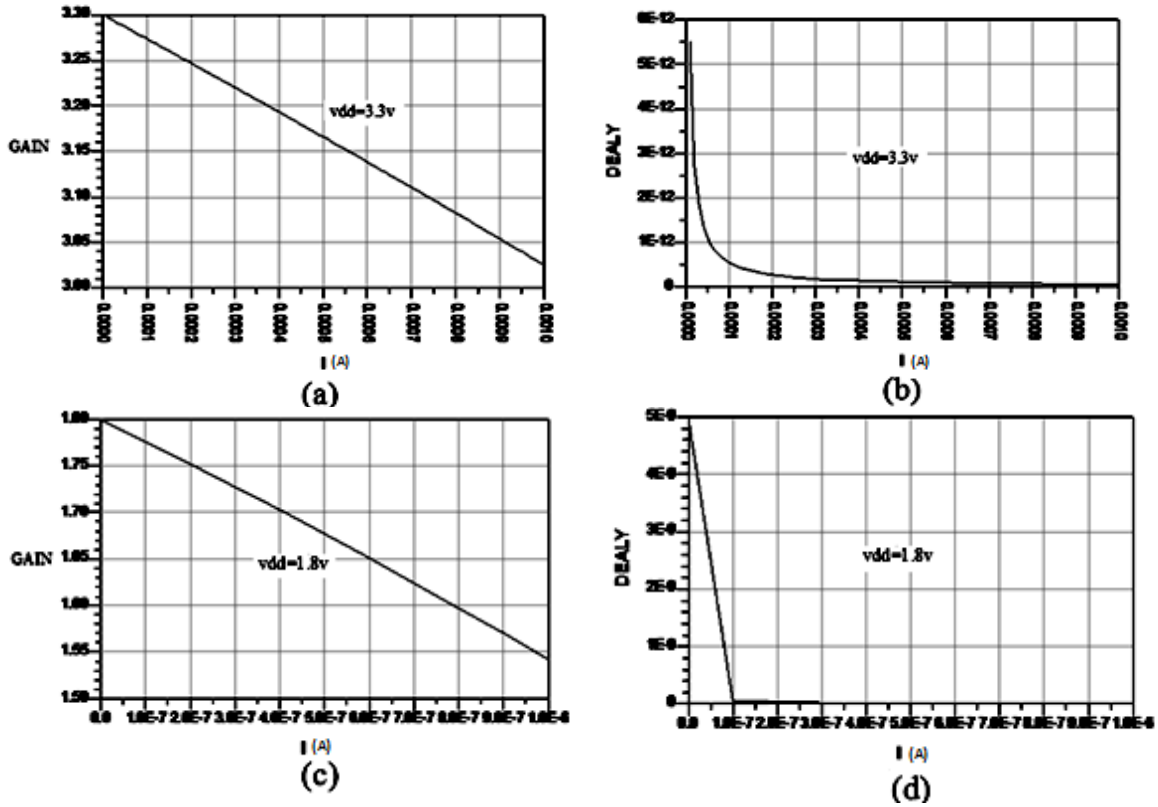
XOR GATE	Vdd=1.8v			Vdd=3v		
	Cmos	MCML (I=1mA)	MCML (I=1uA)	Cmos	MCML (I=1mA)	MCML (I=1uA)
Delay(sec)	$2.61e^{-11}$	$2.2e^{-11}$	$2.1e^{-11}$	$1.29e^{-11}$	$8.4e^{-11}$	$8.021e^{-12}$
PDP(joule)	$1.41e^{-14}$	$7.05e^{-14}$	$8.12e^{-17}$	$3.795e^{-14}$	$9.2e^{-14}$	$1.29e^{-16}$
Power Dissipated (watt)	0.002	$4.45e^{-4}$	$4.7e^{-7}$	0.010	$7.25e^{-4}$	$8.15e^{-7}$

Table III Performance measures for MCML and Cmos DLATCH logic gates

DLATCH GATE	Vdd=1.8v			Vdd=3v		
	Cmos	MCML (I=1mA)	MCML (I=1uA)	Cmos	MCML (I=1mA)	MCML (I=1uA)
Delay (sec)	$3.92e^{-10}$	$1.69e^{-11}$	$1.1e^{-11}$	$1.878e^{-11}$	$2.584e^{-11}$	$7.1e^{-12}$
PDP (joul)	$1.37e^{-14}$	$9.08e^{-15}$	$6.6e^{-18}$	$3.721e^{-14}$	$1.108e^{-14}$	$1.2e^{-17}$
Power Dissipated(watt)	0.0012	0.001	$8.5e^{-7}$	0.005	0.0015	$1.55e^{-6}$

b. Effect of bias current (I) of MCML Inverter:

The gain and delay for MCML inverter versus bias current (I) are shown in fig(6) for 0.18cmos technology and different supply voltages.It can be observed that when the I is scaled up, the gainand the delay will decrease.



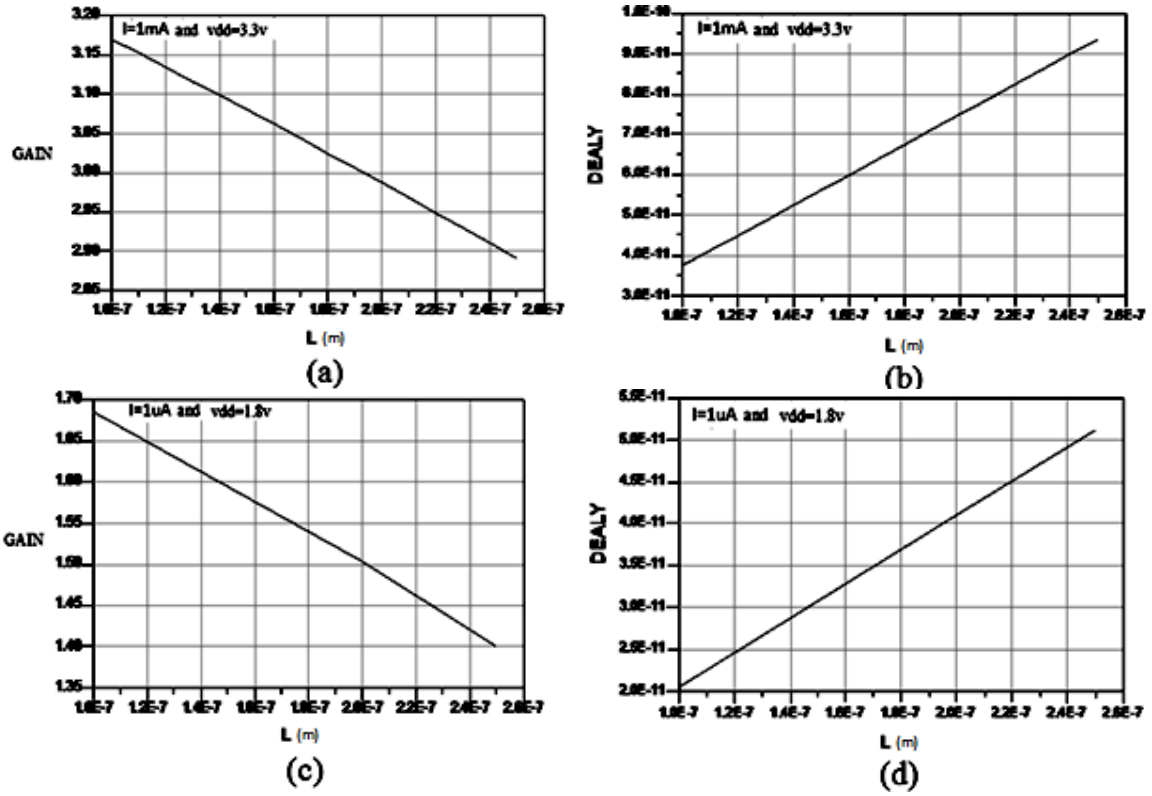
Fig(6) Gain and delay versus bias current I(A)plot of MCML Inverter for different supple voltage (vdd)

c. Effect of length size for Pmos load and Nmos differtional transistor:

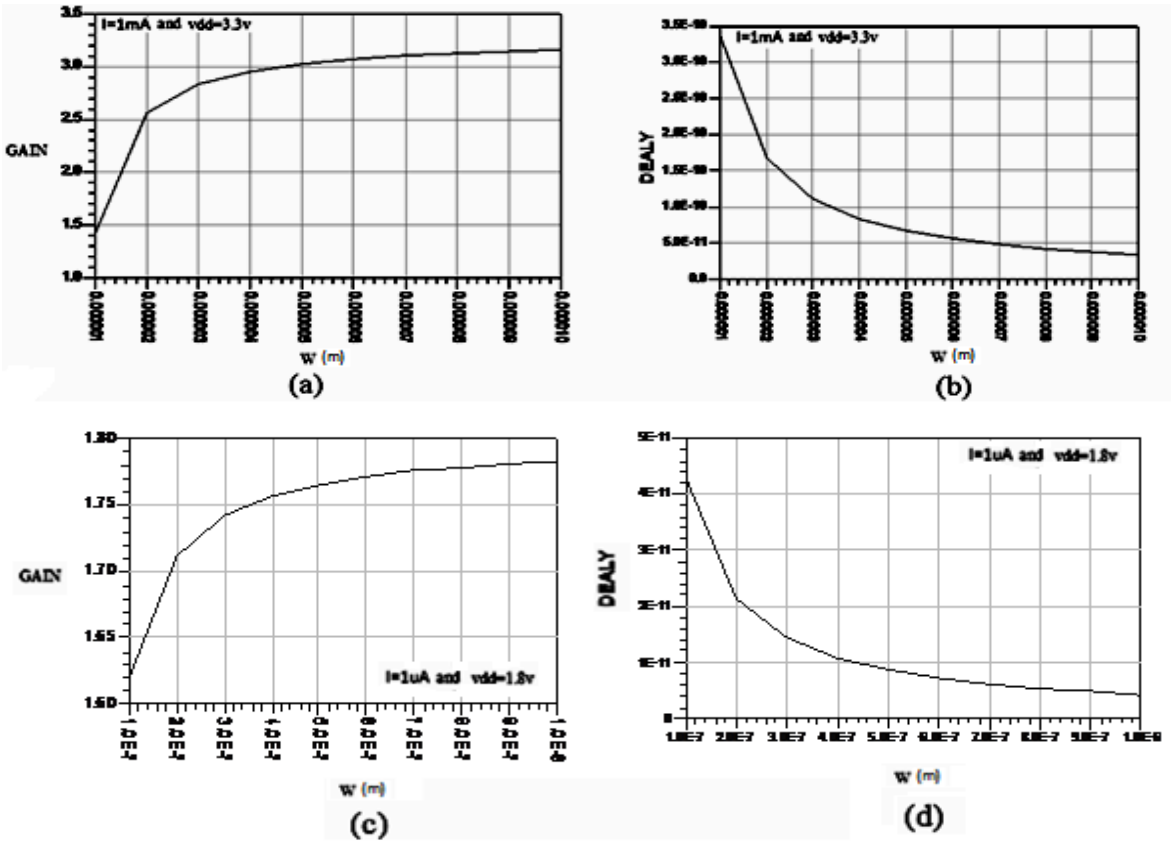
The gain and delay for MCML inverter versus length size for Pmos load and Nmos differential transistor are shown in fig(7) for 0.18cmos technology at different supply voltage and different bias currents(I).It can be observed that when the L is scaled up, the gain decreases but the delay increases.

d. Effect of width size for Pmos load:

The gain and delay for MCML inverter versus width size for Pmos load transistor are shown in fig(8) for 0.18cmos technology at different supply voltage and different bias current(I).It can be observed that when theW is scaled up, the gain willincreasebut the delaywill decrease.



Fig(7) Gain and delay versus length size L(m) plot of MCML Inverter for different supple voltage (vdd) and current bias(I)



Fig(8) Gain and delay versus width size W(m) plot of MCML Inverter for different supple voltage (vdd) and current bias (I)

VI. Conclusion:

This paper presents performance comparison of static CMOS logic gates and MCML logic gates at 0.18µm technology node. All the simulations have been done on Advanced Design System(ADS) software. The simulation results show that MCML logic gates are advantageous over CMOS logic gates in the applications where delay is the main concern. And in the sub-threshold region of operation, both the gate topologies have comparable PDP. The simulation results show the advantage of MCML gates over the CMOS gatesfor high speed low power applications. The behavior of MOS Current-Mode Logic gate under conditions of reduced power supply voltage has been investigated, and it was shown that the operating voltage can be reduced by at least 54% from its nominal value without deteriorating the gate operation. From the results shown it is seen that the MCML logic circuits reveal high efficiency and good performance at low power and high speeds which makes them to be more capable for application in the integrated circuits with high density.

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